REMARKS

Claims 1-20 are currently pending. By this Amendment, claims 1, 5, 8, 11, 15 and 18 have been amended for clarification of the claimed invention, without acquiescence in cited basis for rejection or prejudice to pursue in a related application. The support for these amendments can be found at least in paragraph [0033], Figs. 2-5 and the claims of the originally filed specification. No new matter has been added. The Examiner clarified in a telephone voicemail message on February 9, 2009, that the Office Action dated November 24, 2008 is a Non-Final Office Action. The paragraphs in the Conclusion of Office Action dated November 24, 2008 stating "this action is made final" is incorrect.

Claim Rejections Under 35 U.S.C. §112

Claims 1-20 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully disagrees. The claims have been amended to clarify the invention. Thus, this rejection is now moot.

For at least the foregoing reasons, Applicant respectfully requests that the § 112, second paragraph, rejections for claims 1 and 11, and their respective dependent claims, be withdrawn.

Claim Rejections Under 35 U.S.C. §103

Claims 1-9 and 11-19 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Masatake (JP 2003-202362) in view of Jaramillo et al. (10 Tips for Successful Scan Design: Part two, February 17, 2000, ednmag.com, pp. 77-90). Applicant respectfully traverses.

Independent claim 1 recites the following limitations:

scanning a first test data from an input pin into a first scan chain during a first state of a clock cycle to test the integrated circuit;

scanning a second test data from the input pin into a second scan chain during a second state of the clock cycle to test the integrated circuit; and

associating a lockup register with a beginning or ending circuit element of the first or second scan chains, wherein a design rule for the act of associated the lockup register with the first or second scan chains associated with the lockup register are based at least in part upon a clock waveform; wherein a clock signal

of the clock cycle is input to the first scan chain and the second scan chain during testing. (Emphasis added).

Applicant respectfully submits that Masatake does not disclose or suggest at least the feature of "associating a lockup register with a beginning or ending circuit element of the first or second scan chains, wherein a design rule for the act of associated the lockup register with the first or second scan chains associated with the lockup register are based at least in part upon a clock waveform" (emphasis added). Specifically, Masatake disclose only a selector 3 associated with the beginning of a scan chain 12. As can be seen by Drawing 1 of Masatake, the selector 3 associated with scan chain 11 merely selects either a positive clock or a negative clock. The claimed invention explicitly recites a design rule for the act of associating based at least in part upon a clock waveform. The support for this feature can be found in [27]-[33]. Masatake is silent with respect to the design rule for associating as claimed. Therefore, Masatake does not disclose or suggest at least "associating a lockup register with a beginning or ending circuit element of the first or second scan chains, wherein a design rule for the act of associated the lockup register with the first or second scan chains associated with the lockup register are based at least in part upon a clock waveform."

Applicant respectfully submits that Jaramillo does not disclose or suggest at least the feature of "associating a lockup register with a beginning or ending circuit element of the first or second scan chains, wherein a design rule for the act of associated the lockup register with the first or second scan chains associated with the lockup register are based at least in part upon a clock waveform" (emphasis added). Jaramillo discloses a scan chain with mixing flip-flops (Fig. 3). Fig. 3 of Jaramillo also discloses a lockup latch. Specifically, Jaramillo discloses on page 83 first paragraph of the second column: "Whenever a falling-edge-triggered flip-flop follows a rising-edge-triggered flip-flop in a scan chain, you must insert a lockup latch between them." Therefore, Jaramillo teaches a design strategy of when must one insert the lockup latch between falling-edge-triggered flip-flop and the rising-edge-triggered flip-flop in a scan chain. Jaramillo inserts a lockup latch to prevent data from shifting through both flip-flops in one clock cycle and places falling-edge-triggered flip-flops at the beginning of the scan chain for each block. Jaramillo is silent with respect to the design rules for associating based at least in part upon clock waveform. Inserting a lockup latch between two kinds of flip-flops is not the same as a design rule for associating based at least in part upon a clock waveform. Therefore, Jaramillo also does not disclose or suggest at least

"associating a lockup register with a beginning or ending circuit element of the first or second scan chains, wherein a design rule for the act of associated the lockup register with the first or second scan chains associated with the lockup register are based at least in part upon a clock waveform."

For at least these reasons, it is respectfully submitted that Masatake and Jaramillo, singly or in combination, does not teach or suggest the invention <u>as a whole</u>. For at least these same reasons, it is respectfully submitted that claims 1 and 11, as amended, are not obvious, and the rejection should be withdrawn.

Since the remaining claims respectively depend from these independent claims, these dependent claims are considered allowable over this reference for at least the same reasons as discussed above.

Claims 7, 10, 17 and 20 were rejected under 35 U.S.C. §103(a) as unpatentable over Masatake in view of Jaramillo et al. and Morton (US 2004/0078741).

However, Applicant respectfully traverses these rejections under 35 U.S.C. §103(a) for at least the reasons as set forth above because Morton was also not cited and fails to disclose or suggest at least the feature of "associating a lockup register with a beginning or ending circuit element of the first or second scan chains<u>, wherein a design rule for the act of associated the lockup register with the first or second scan chains associated with the lockup register are based at least in part upon a clock waveform</u>" (emphasis added).

Since claims 7, 10, 17 and 20 respectively depend from independent claims 1 and 11, these dependent claims are considered allowable over the cited references for at least the same reasons as discussed above and/or for at least their dependence on the independent claims.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

To the extent that any arguments and disclaimers were presented to distinguish prior art, or for other reasons substantially related to patentability, during the prosecution of any and all parent and related application(s)/patent(s), Applicant(s) hereby explicitly retracts and rescinds any and all such arguments and disclaimers, and respectfully requests that the Examiner re-visit the prior art that such arguments and disclaimers were made to avoid.

The Commissioner is authorized to charge any fees due in connection with the filing of this document to Vista IP Law Group's Deposit Account No. 50-1105, referencing billing number CA7035962001. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Vista IP Law Group's Deposit Account No. 50-1105, referencing billing number CA7035962001.

Respectfully submitted,

Dated: _____ February 23, 2008 _____   By: _____ /Jasper Kwoh/ _____
Jasper Kwoh
Registration No. 54,921

Vista IP Law Group LLP   for
1885 Lundy Avenue,   Peter C. Mei
Suite 108   Registration No. 39,768
San Jose, CA 95131
Telephone: (408) 321-8663